REMARKS

In the Office Action dated September 22, 2004, the Examiner has ***finally rejected*** claims 1-3 and 5-19 pending in the application on the basis of new grounds of rejection and newly cited art. Applicant respectfully requests reconsideration and withdrawal of the finality of the rejection of the Office Action dated September 22, 2004.

A good and sufficient reason why the present response is necessary and was not earlier presented is that an entirely new reference has been cited in the present final rejection dated September 22, 2004 (37 §CFR 1.116 (c)). The new reference is U.S. Patent Number 6,451,676 to Wurzer, et al. ("Wurzer") which is for the first time brought to Applicant's attention by means of the present ***final rejection*** dated September 22, 2004. The new reference, i.e., Wurzer, was not cited in the present application prior to the instant final rejection. Since Wurzer is a reference upon which the Examiner has now relied, Applicant believes that it would be manifestly unfair for the Patent Office not to consider Applicant's arguments which are necessitated due to the newly cited reference, Wurzer. As such, a good and sufficient reason exists, as required by 37 CFR §1.116(c), for considering Applicant's present response and withdrawing the finality of the present Office Action.

A. Rejections of Claims 1-3 and 5-19 under 35 USC §103(a)

The Examiner has rejected claims 1-3 and 5-19 under 35 USC §103(a) as being unpatentable over U.S. Patent Number 5,963,810 to Gardner, et al. ("Gardner"), U.S.

Patent Number 6,124,158 to Dautartas, et al. ("Dautartas"), U.S. Patent Number 5,994,192 to Chen ("Chen"), "admitted prior art," U.S. Patent Number 6,369,430 to Adetutu, et al. ("Adetutu"), and U.S. Patent Number 6,451,676 to Wurzer, et al. ("Wurzer"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by independent claims 1 and 12, is patentably distinguishable over Gardner, Dautartas, Chen, Adetutu, and Wurzer.

Various embodiments according to the present invention, as defined by independent claims 1 and 12, involve depositing a first ultra-thin nitride film by atomic layer deposition (ALD) on a semiconductor substrate that comprises a silicon-on-insulator (SOI) wafer (claim 12), depositing a high-k material on the first ultra-thin nitride film, depositing a second ultra-thin nitride film on the high-k material by ALD, and depositing a gate material on the second ultra-thin nitride film, wherein the gate material comprises polysilicon-germanium (poly-SiGe).

One embodiment provides a nitride/high-k material/nitride gate dielectric stack, where the nitride films are deposited by ALD to achieve thicknesses in a range of 1 to 2 atomic layer(s), and a gate electrode comprising a gate material including polysilicon-germanium, which is formed over the gate dielectric stack.

Consequently, a high-k dielectric gate insulator is achieved, where the first and second nitride films advantageously increase thermal stability by preventing metal from the high-k material from diffusing into the semiconductor substrate and the polysilicon-germanium gate material, respectively, during subsequent high temperature processes.

Therefore, embodiments according to the present invention advantageously achieve a high-k dielectric gate insulator having good thermal stability that can be combined with gate material comprising polysilicon-germanium. Additionally, various embodiments achieve a high-k dielectric gate insulator that advantageously provides a reduction of direct tunneling current flow in a semiconductor device, such as a MOSFET. Further, various embodiments advantageously achieve a high-k dielectric gate insulator that can be situated on a semiconductor substrate that can comprise an SOI wafer.

In contrast to the present invention as defined by independent claims 1 and 12, the cited art does not teach, disclose, or suggest depositing a first ultra-thin nitride film by ALD on a semiconductor substrate that comprises a silicon-on-insulator (SOI) wafer (claim 12), by atomic layer deposition, depositing a high-k material on the first ultra-thin nitride film, depositing a second ultra-thin nitride film on a high-k material by ALD, and depositing a gate material on the second ultra-thin nitride film, wherein the gate material comprises polysilicon-germanium (poly-SiGe). Gardner specifically discloses forming high permittivity layer 305 over thin nitride layer 303 and forming a nitride capping layer over high permittivity layer 305 prior to form gate electrode layer 307. See, for example, column 5, lines 52 and 53, column 6, lines 13-15, and Figure 3C of Gardner.

Referring to Gardner, nitrogen-bearing layers, i.e. thin nitride layer 303 and the nitride capping layer, formed between high permittivity layer 305 and the substrate or gate electrode layer 307, serve to inhibit oxidation of high permittivity layer 305 during subsequent processing. See, for example, Gardner, column 5, lines 13-24. However,

Gardner fails to teach, disclose, or even suggest forming thin nitride layer 303 and nitride capping layer using ALD.

Additionally, Gardner fails to teach, disclose, or suggest depositing a first ultra-thin nitride film by ALD on a semiconductor substrate that comprises an SOI wafer, as set forth in independent claim 12. In fact, Gardner fails to even mention an SOI wafer or provide any motivation for utilizing a semiconductor substrate that comprises an SOI wafer. Further, Gardner fails to teach, disclose, or suggest the deposition of a gate material including polysilicon-germanium on an ultra-thin nitride film using ALD.

Dautartas fails to cure the deficiencies of Gardner. Dautartas does make mention of an ALD process that is particularly advantageous for the low temperature deposition of gate dielectric materials, such as aluminum oxide, from an organic precursor, particularly trimethyl-aluminum, as well as other dielectrics deposited from carbon-containing precursors, such as tantalum oxide from tantalum alcoholate (pentaethoxytantalum). Dautartas, column 3, lines 7-14. Nevertheless, Dautartas does not teach, disclose, or suggest depositing a gate material on an ultra-thin nitride film that has been deposited using an ALD technique, where the gate material comprises polysilicon-germanium. Further, Dautartas fails to even mention a gate material comprising polysilicon-germanium. In addition, Dautartas fails to teach, disclose, or even suggest depositing an ultra-thin nitride film on a substrate comprising an SOI wafer, as recited in independent claim 12. In fact, Dautartas fails to even mention a substrate comprising an SOI wafer.

Dautartas does not disclose, teach, or suggest the process steps of independent claims 1 and 12. Furthermore, there is no teaching or suggestion to combine or modify Dautartas. Therefore, Dautartas, singly or in combination with other art of record, does not disclose, teach or suggest the present invention as defined by independent claims 1 and 12.

Furthermore, Chen does not cure the deficiencies of Gardner and Dautartas. The Examiner asserts that Chen teaches the use of photoresist as part of the patterning process as required in claims 10, 18, and 19. However, Chen fails to teach, disclose, or suggest depositing a gate material on an ultra-thin nitride film that has been deposited using an ALD technique, where the gate material comprises polysilicon-germanium. Moreover, Chen fails to teach, disclose, or suggest depositing an ultra-thin nitride film on a substrate comprising a SOI wafer, as specified in independent claim 12.

Chen does not disclose, teach, or suggest the process steps of independent claims 1 and 12. Furthermore, there is no teaching or suggestion to combine or modify Chen. Therefore, Chen, singly or in combination with other art of record, does not disclose, teach or suggest the present invention as defined by independent claims 1 and 12.

Adetutu does not cure the deficiencies of Gardner, Dautartas, and Chen. Adetutu is cited by the Examiner as teaching a substrate comprising a SOI wafer, as recited in independent claim 12 and dependent claim 2. However, Adetutu does not provide any motivation for depositing an ultra-thin nitride film on a substrate comprising an SOI wafer, as specified in independent claim 12. Furthermore, Adetutu fails to teach,

disclose, or suggest depositing a gate material on an ultra-thin nitride film that has been depositing using an ALD technique, where the gate material comprises polysilicon-germanium.

Adetutu does not disclose, teach, or suggest the process steps of independent claims 1 and 12. Furthermore, there is no teaching or suggestion to combine or modify Adetutu. Therefore, Adetutu, singly or in combination with other art of record, does not disclose, teach or suggest the present invention as defined by independent claims 1 and 12.

Wurzer fails to cure the deficiencies of Gardner, Dautartas, Chen, and Adetutu. Wurzer is directed to a method for setting the threshold voltage of a MOS transistor. The Examiner asserts that Wurzer discloses forming a gate material comprising polysilicon-germanium. Nevertheless, Wurzer provides no motivation for combining Wurzer with Gardner. Further, Wurzer does not even suggest depositing a gate material on the second ultra-thin nitride film.

Wurzer does not disclose, teach, or suggest the process steps of independent claims 1 and 12. Furthermore, there is no teaching or suggestion to combine or modify Wurzer. Therefore, Wurzer, singly or in combination with other art of record, does not disclose, teach or suggest the present invention as defined by independent claims 1 and 12.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by independent claims 1 and 12, is not taught, disclosed, or suggested by the art of record. Thus, independent claims 1 and 12 are patentably

distinguishable over the art of record. As such, the claims depending from independent claims 1 and 12 are, *a fortiori*, also patentable for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. Conclusion

Based on the foregoing reasons, the present invention, as defined by independent claims 1 and 12, and the claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, outstanding claims 1-3 and 5-19 are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early Notice of Allowance directed to all claims 1-3 and 5-19 remaining in the present application is respectfully requested.

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Respectfully Submitted,
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